REMARKS

Claims 1-22 are pending in which claims 9-22 are allowed and claims 1-8 were objected to in the Ex parte Quayle Office Action.

Preliminarily, paragraph **[0028]** is amended to replace the incorrect reference number 105 with the correct reference number 103 for the MARCTRL pin. As shown in FIG. 1 and as referenced throughout the application as filed, the MARCTRL pin is pin 103 rather than pin 105, which instead refers to the OFS+ pin. Applicant submits that this is a formality error which does not add new matter and requests approval of this amendment.

Furthermore, the reference number 201 and leader line identifying the adder 201, which receives and adds the voltages VMARG and VREF and which provides the voltage VRM, are missing in FIG. 2. The adder 201 is initially referenced on the last line of page 14 in paragraph **[0028]** and again on the top line of page 15 in the same paragraph of the application as filed. Coincidentally, this same paragraph **[0028]** is repeated and amended herein on page 2 of this amendment. A replacement sheet for FIGS 1 and 2 is included with FIG. 2 including the change in which the missing reference designation 201 and leader line are added to identify the adder 201. An Annotated sheet is also included showing the change in red. Applicant requests approval of this drawing change.

In the Office Action, it was stated that there appeared to be some confusion with the connection order of the first and second margining nodes and surrounding components. It was further stated that claim 1 appears to define the circuit in "mode B" whereas claim 2 appears to define the circuit in "mode A."

Applicant respectfully submits that claim 1 does not define the circuit in any particular "mode" as referenced in the Office Action. Although the claims are not limited to the particular

embodiments shown in the Figures, it is assumed that the reference to modes A and B is in reference to the A and B portions and nodes of FIGS 1 and 2. Thus, as shown in FIG. 1, "mode A" references the MARCTRL pin 103 being pulled high so that switches SW1 and SW2 select the A positions and the amplifiers A1 and A2 are selected, and "mode B" references the MARCTRL pin 103 being pulled low so that switches SW1 and SW2 select the B positions and the amplifiers A3 and A4 are selected. In that particular embodiment illustrated, note that in "mode A" the amplifier 111 drives the OFS- pin 107 to regulate the voltage at the OFS+ pin 105 to VREF, whereas in "mode B" the same amplifier 111 drives the OFS+ pin 105 to regulate the voltage at the OFS- pin 107 to VREF. Continuing this same example, the "first margining resistor" reads on the resistor RMARG and the "first amplifier circuit" reads on the amplifier 111 and supporting circuitry (e.g., transistor Q1). Yet while claim 1 recites that the margining resistor is coupled between "first and second margining nodes", claim 1 does not specify which node is which. Thus, if the margining nodes read on the OFS+ and OFS- pins, *either one* of these nodes/pins could be the first or the second margining node. Further, the "first offset resistor" reads on *either* resistor ROFS+ or ROFS-, depending on the selected mode, and the "second amplifier circuit" reads on *either* the amplifier pair A1/A2 or A3/A4, depending on the selected mode.

Claim 2 also is not intended to limit to either mode. Nonetheless, claim 2 does not appear to be consistent with claim 1 as noted by the Examiner. Since claim 1 recites that the first amplifier drives current to the first margining node to establish a first reference voltage at the second margining node, the current path of the current device should be coupled to the <u>first</u> margining node rather than the second margining node as originally claimed. Claim 2 is amended herein to recite that the current path of the current device is coupled to the first

margining node. Applicant submits that claim 2 is now consistent with claim 1. And Applicant further notes that neither claim 1 nor 2 is specifically limited to either of the "modes" as suggested in the Office Action. Claim 4 does include select logic with "up and down states" and thus references two states or modes, but does not specify which margining node is which but only that both are included in the circuit.

Applicant respectfully submits, therefore, that claims 1-8 now employ consistent terminology. Applicant requests withdrawal of this objection.

It was further stated that the phrase "reference voltage" described voltages at nodes VREF, OFS+ and OFS-, which are three different voltages at three different circuit locations and should have individual designations.

Applicant respectfully traverses this objection. In claim 1, the reference voltage is a predetermined or selected voltage level and does not have to be a particular node; and the reference voltage could be applied to any one or more nodes. Claim 1 recites that the first amplifier circuit *establishes* the reference voltage at the second margining node, and that the feedback circuit adjusts a set point voltage *based on* the reference voltage *and* a first margining current. Although the specific embodiment shown in FIGS 1-3 do show a VREF node (with voltage level of VREF), the present invention contemplates alternative embodiments in which amplifier circuitry or the like simply drives the specified nodes based on an arbitrary reference voltage *without actually employing a node at that same reference voltage*. Such is possible and, in fact, rather common in the industry and there is no basis for limiting the claims to any particular design configuration.

As noted above in the particular embodiment of the Figures, either one of the OFS+ or OFS- pins are driven to the same voltage level VREF depending upon the particular "mode" (A

or B). Claim 1 is not limited to either mode. And claim 4 reads on either or both modes in which the select logic effectively reverses the output and feedback input of the amplifier circuit between the first and second margining nodes depending upon whether it is in the up or down states. In this case, the reference voltage is *established* at either one of the first and second margining nodes depending upon the state of the select logic. In the particular embodiment disclosed, the amplifier 111 controls Q1 to regulate one of the nodes OFS+ or OFS- to VREF applied at an input of the amplifier 111 depending upon the selected mode or state (e.g., up or down margining).

In the particular embodiments shown and described, the same VREF signal is employed to at the input of the amplifier 111, and also to set the nominal level of the output voltage without margining (e.g., applied to the adder 201 in FIG. 2 or applied to the base of transistor 301 in FIG. 3). While it is convenient to employ the same reference voltage level, the present invention is not limited to the same reference voltage since they serve two different albeit related functions. Thus, claim 1 is amended to recite that the first amplifier circuit drives current to the first margining node to establish a first reference voltage at the second margining node, whereas the feedback circuit adjusts the set point voltage based on a second reference voltage and the first margining current. Claim 2 is amended in accordance with amended claim 1 in which the first amplifier circuit includes an amplifier having an input receiving the first reference voltage. Claim 3 is amended to recite a summing circuit which adds the second reference voltage to a second margining voltage to adjust the set point voltage. And claim 4 is amended to recite that the feedback circuit adjusts the set point voltage based on the second reference voltage and the first and second margining currents. Applicant requests approval of these amendments.

CONCLUSION

Applicant respectfully submits that for the reasons recited above and for various other reasons, the objections have been overcome and should be withdrawn. Applicant respectfully submits therefore that the present application is in a condition for allowance and reconsideration is respectfully requested. Should this response be considered inadequate or non-responsive for any reason, or should the Examiner have any questions, comments or suggestions that would expedite the prosecution of the present case to allowance, Applicants' undersigned representative earnestly requests a telephone conference.

Respectfully submitted,

Date: June 9, 2005

By: 

Gary R. Stanford
Reg. No. 35689

Amendments to the Drawings:

The attached sheet of drawings includes a change to FIG. 2. The replacement sheet, which includes FIGS 1 and 2, replaces the original sheet including FIGS 1 and 2. The annotated sheet shows, in FIG. 2, the change in which the missing reference designation 201 and leader line are added to point to the adder 201. The adder 201 is initially referenced on the last line of page 14 in paragraph [0028] and again on the top line of page 15 in the same paragraph of the application as filed. Coincidentally, this same paragraph [0028] is repeated and amended herein on page 2 of this amendment.

Attachment: Replacement Sheet

Annotated Sheet Showing Changes

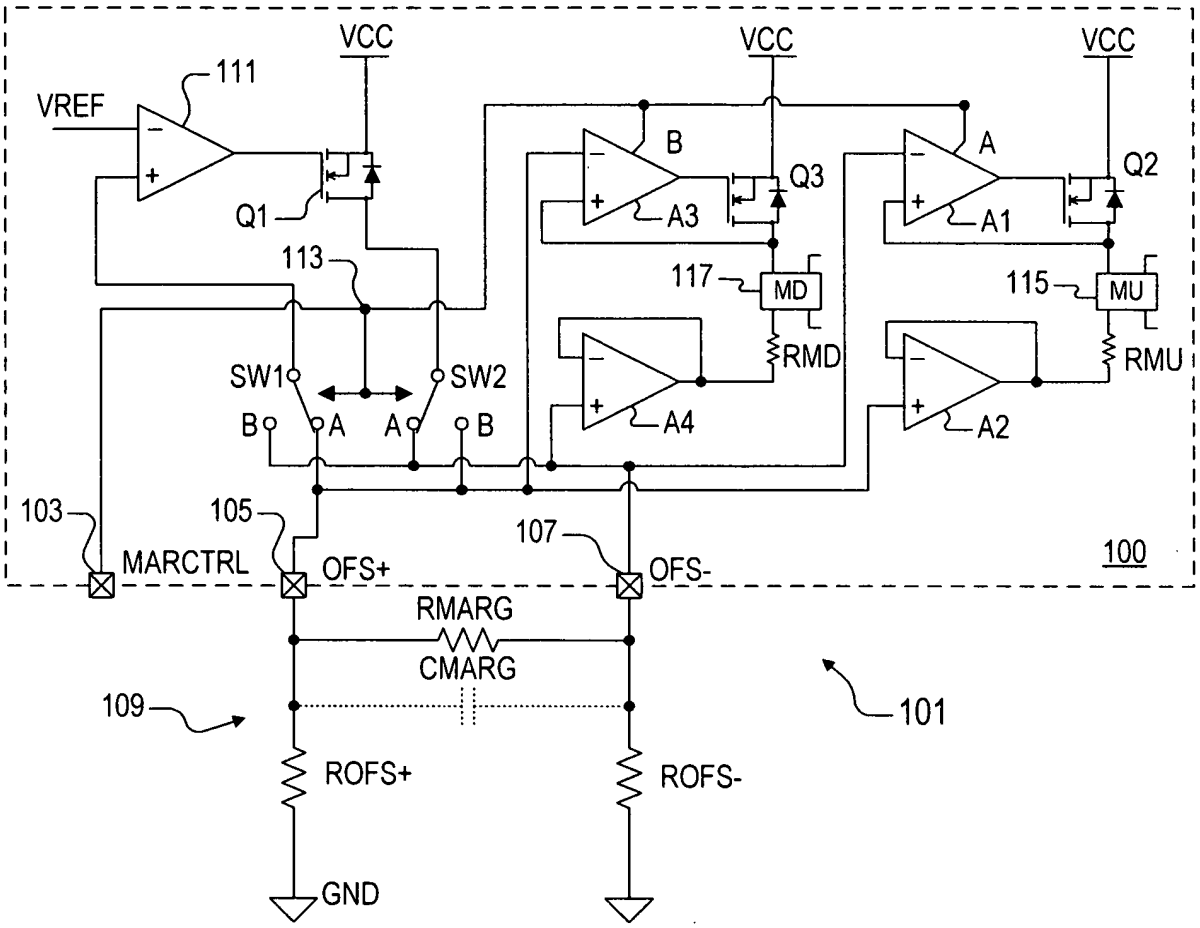
VCC
VCC
VCC
VREF
111
Q1
B
A3
Q3
A
A1
Q2
113
117
MD
115
MU
RMD
RMU
SW1
SW2
B
A
A
B
A4
A2
103
105
107
MARCTRL
OFS+
OFS-
100
RMARG
CMARG
109
101
ROFS+
ROFS-
GND

FIG. 1

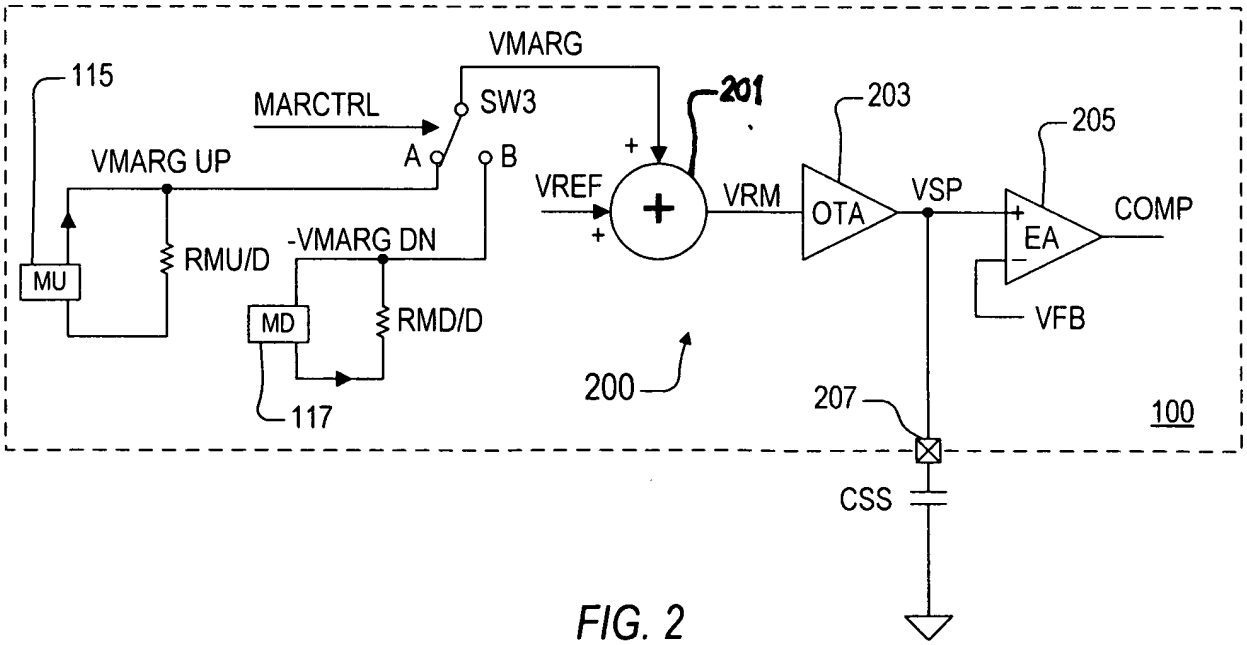
VMARG
115
MARCTRL
SW3
201
203
205
VMARG UP
A
B
+
VREF
VRM
OTA
VSP
EA
COMP
MU
RMU/D
-VMARG DN
MD
RMD/D
VFB
200
117
207
100
CSS

FIG. 2